TRS-80/SYSTEM-80 EXPANSION INTERFACE
USER MANUAL & SYSTEM REFERENCE

MICRO-80 P/L
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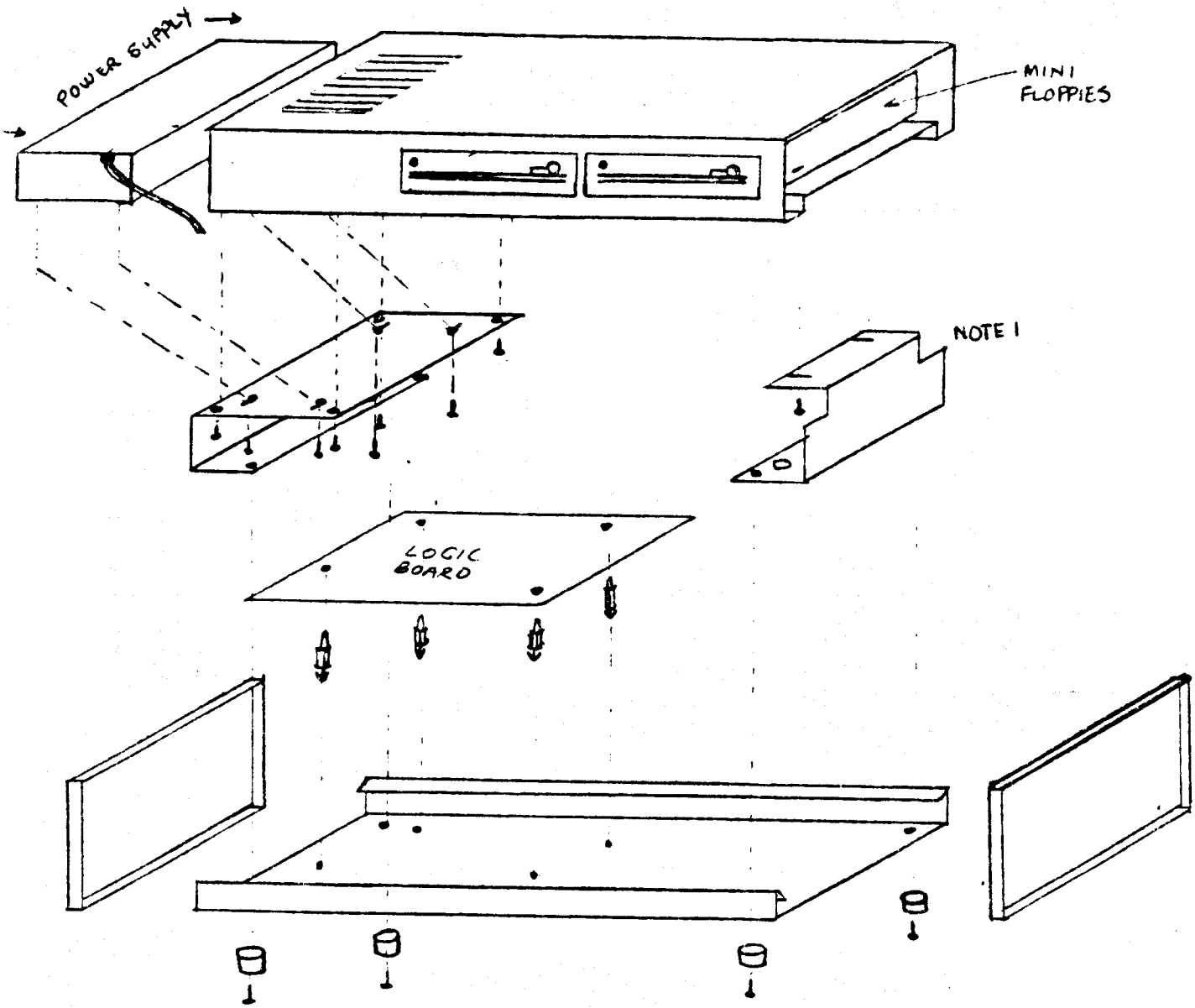


Fig 1.0 Expansion case exploded view.

Note 1: Left bracket is the same as right bracket in non disk units.

1.0 INTRODUCTION.

The Micro-80 Expansion interface was designed to replace both the Tandy and Dick Smith expansion interfaces for the TRS-80 and SYSTEM-80 computers. The Micro-80 interface offers greater reliability and more recent technology. The original TRS-80 interface had many problems such as; mains interference because of overtaxed power supply, bad connections because of corroding card edges, unreliable memory and failing RS232 boards due to warped connector blocks to name just a few. With these problems in mind a completely new interface has been designed to overcome these faults.

The Micro-80 interface has headers for all I/O ports to give reliable connections without the posibility of corrosion. The latest generation of high speed (150 nS) CMOS rams (8K x 8 Bits) are used, to avoid having to rely on CAS and MUX signals from the keyboard unit. These signals are passed to the expansion interface through a ribbon cable and are degraded by the time they arrive at the interface. Another benefit of using CMOS rams is their low power consumption which presents the power supply with much less load which in turn should decrease sensitivity to mains interference. The interface has been designed to be compatible with both the SYSTEM-80 and TRS-80 computers. The printer port is decoded to address 37E8H and port FDH to suit both machines. The RS232 section is decoded to TRS-80 conventions because all RS-232 driver software is written for the TRS-80. SYSTEM-80 owners previously had problems using this software. The interface can easily be modified for either machine by removal or insertion of one IC and one jumper wire on the PC board.

2.0 INSTALLATION.

The Expansion unit will have been supplied to you set up for connection to the TRS-80 or SYSTEM-80 computers depending on which unit you ordered. This should be verified by looking at the sticker on the bottom of the expansion case where this is identified. If the unit is set up incorrectly refer to the "SYSTEM-80/TRS-80 conversion circuit" section in the technical section of this manual for conversion details of the expansion interface.

Refer to Illustration 2.1 or 2.2 for details on how to connect the computer to the expansion interface. Note that the I/O interface cables are different from the standard SYSTEM-80 or TRS-80 cables because the MICRO-80 interface has headers instead of card edges. This means that the correct cables will have to be ordered from MICRO-80 or existing cables must be modified. You will find that the greatly increased reliability of headers compared to tin coated card edges makes this difference worthwhile.

When all peripherals are plugged in (see following sections) apply power first to peripherals such as printer, disk drives and modems, then apply power to the expansion unit and finaly to the computer. Note that the power point selected for the computer and peripherals must be used only for this purpose and not for anything else, the more load applied to a power point the more chance of mains interference to the computer and hence a degradation of reliability. If you live in a building with old wiring or in an industrial area you may need a good quality mains filter or in extreme conditions a mains conditioner. Good mains filters are not cheap, beware of cheap filters as these are a waste of money. If a filter is purchased make sure that it has been designed for computer systems, like the "MAINS MUFFLER" manufactured by Sigtronic Industries P/L in Sydney which has seperate filtered sockets for peripherals and the computer.

Finally note that in this manual the term TRS-80 and SYSTEM-80 may be used interchangeably. Unless it is specificaly mentioned otherwise, everything in this manual relating to the TRS-80 applies to the SYSTEM-80.

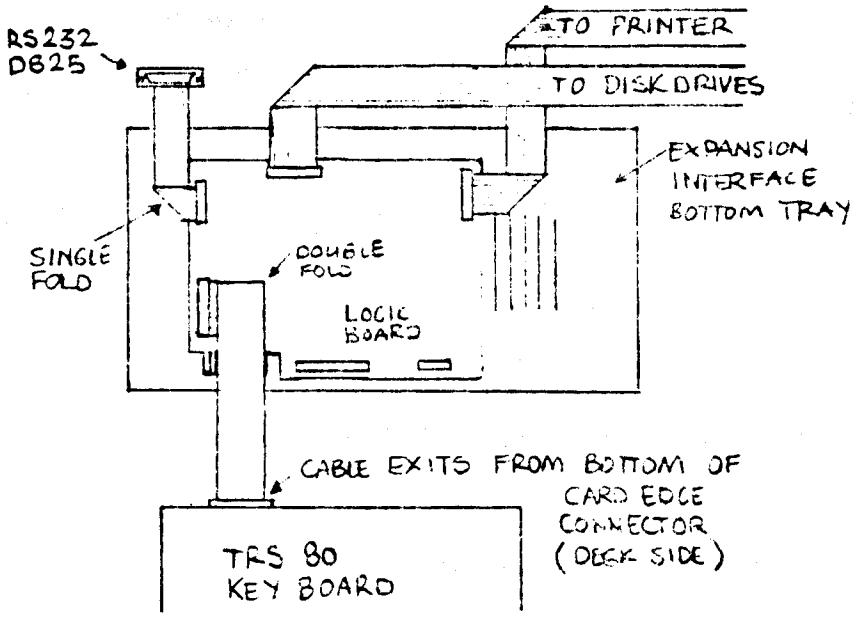

RS232
D825
TO PRINTER
TO DISK DRIVES
EXPANSION
INTERFACE
BOTTOM TRAY
SINGLE
FOLD
DOUBLE
FOLD
LOGIC
BOARD
CABLE EXITS FROM BOTTOM OF
CARD EDGE
CONNECTOR
(DESK SIDE)
TRS 80
KEY BOARD

FIG 2.1

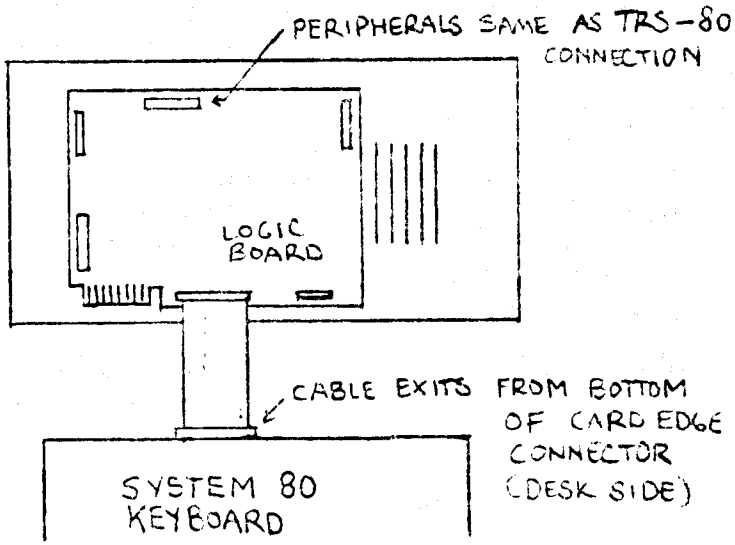

PERIPHERALS SAME AS TRS-80
CONNECTION
LOGIC
BOARD
CABLE EXITS FROM BOTTOM
OF CARD EDGE
CONNECTOR
(DESK SIDE)
SYSTEM 80
KEYBOARD

FIG 2.2

3.0 FLOPPY DISK CONTROLLER.

The standard expansion interface comes with a single density controller (1771). Any double density adaptor can be used with this unit to take advantage of the greater storage of double density disk drives and DOS's. The recommended double density adaptors are the LNW 5/8 doubler or the MICRO-80 doubler. These units have a Phased Lock Loop data separator. Most other units have counter type separators and are inferior. See technical sections 10.5 and 10.7 for more information on the FDC.

Note diagram 2.1 for floppy disk drive connection.

4.0 RS232 INTERFACE.

The RS232 interface can be used to drive serial printers, modems and terminals. All of these applications of course need the appropriate software to be written or bought. Some RS232 software needs the RS232 configuration jumpers to be configured inside the expansion interface, other software does it all under software control and ignores the jumpers. If the configuration jumpers need to be configured refer to section 4.3. The RS232 port consists of a header on the logic board into which a short cable should be plugged with a DB25 connector.

4.1 RS232 SIGNALS.

PIN No.	DIRECTION.	SIGNAL NAME.	
2	From interface.	TX	(Transmit data).
3	Into interface.	RX	(Receive data).
4	From interface.	RTS	(Ready To Send).
5	Into interface.	CTS	(Clear To Send).
6	Into interface.	DSR	(Data Set Ready).
7	N/A	GND	(Signal Ground).
8	Into interface.	CD	(Carrier Detect).
20	From interface.	DTR	(Data Terminal ready).

The data direction is shown here because manufacturers of RS232 equipment might make any of these signals inputs or outputs, just to confuse the matter. As a general guide printers may use any of the signals TX, RX, GND, DSR and DTR, Modems and terminals may use any of TX, RX, GND, CTS, RTS, CD, DSR and DTR. If you purchase RS232 equipment and you are not completely familiar with RS232 conventions be sure that you make the retailer responsible for making the correct interface cable for you. However to help you, below you will find connection diagrams for several common RS232 devices.

4.2 COMMON RS232 DEVICE CONNECTIONS.

There are basicly 3 different types of RS232 devices you may wish to connect. These are Printers, Modems or Acoustic couplers and Terminals. The most common of each are discussed here and connection diagrams shown.

SENDATA MODEM.

The sendata modem and acoustic coupler is possibly the most common since it is manufactured in Australia. Any other modems should also work with these connections. As you can see this is a straight through connection, a mass termination type ribbon cable with a crimp-on DB25 can be used.

INTERFACE PIN No.	--TO--	MODEM PIN No.
7 (GND)		7 (GND)
2 (TX)		2 (TX)
3 (RX)		3 (RX)
8 (CD)		8 (CD)

EPSON MX-80 TYPE SERIAL PRINTER CONNECTION.

For this example we will use the MX-80 or MX-80 look-alike type serial interface as it represents the most common type printer interface.

INTERFACE PIN No.	--TO--	PRINTER PIN No.
7 (GND)		7 (GND)
2 (TX)		3 (RX)
6 (DSR)		20 (DTR)

RS232 TERMINAL CONNECTION.

This example is for a Televideo terminal but most terminals have the same signals on the same pins, therefore this example can be used for any terminal. NOTE this is also the correct way to connect a cable between two TRS-80's for data transfer.

INTERFACE PIN No.	--TO--	TERMINAL PIN No.
2 (TX)		3 (RX)
3 (RX)		2 (TX)
4 (RTS)		5 (CTS)
5 (CTS)		4 (RTS)
6 (DSR) & 8 (CD)		20 (DTR)
7 (GND)		7 (GND)
20 (DTR)		6 (DSR) & 8 (CD)

RS232 CONFIGURATION JUMPERS.

Some RS232 software needs the RS232 configuration jumpers set to function correctly. The configuration jumpers (Jumper area "E" on the board) are actually plugged into a small 16 pin header at the left bottom edge of the board. The jumper numbers are marked on the board and run right to left from 1 to 8. Each of these jumpers has a function with respect to the RS232 port. (These jumpers are in fact read by the Z80 CPU as an 8 bit port so the significance of the individual jumpers may well vary between different programs. Consult your software manuals.) They are defined as:

JUMPER No. — FUNCTION.

1 — Parity selection.
ON = Odd parity
OFF = Even parity.

2,3 — Word length selection.

J2	J3	WORD LENGTH
ON	ON	5 bits.
ON	OFF	6 bits.
OFF	ON	7 bits.
OFF	OFF	8 bits.

4 — Parity enable jumper.
ON = Parity enabled
OFF = Parity disabled.
If this jumper is off jumper 1 is ignored.

5 — Stop bit selection.
ON = 1 stop bit
OFF = 2 stop bits.

6,7,8 — Baud rate selection.

J6	J7	J8	BAUD RATE.
ON	ON	ON	110
ON	ON	OFF	150
OFF	ON	ON	300
OFF	ON	OFF	600
ON	OFF	ON	1200
ON	OFF	OFF	2400
OFF	OFF	ON	4800
OFF	OFF	OFF	9600

5.0 CLOCK INTERRUPTS.

The expansion interface has an inbuild clock circuit which provides an interrupt to the Z80 every 25mS. Provided that the interrupts are enabled the Z80 will jump to 4012H. It is therefore possible to put a "Jump" to an interrupt service routine at locations 4012H to 4014H. This interrupt service routine could, for instance, increment a counter to provide a real time clock (like TRSDOS does) or any other function like scanning the keyboard to see if the Break key is down. Providing the Z80 interrupts are left on, this would allow a program or function to be aborted without having to scan the BREAK key every time manually. More information can be found in technical section 10.7. and in the address decoding section 9.1 under 37E0H.

6.Ø PARALLEL PRINTER INTERFACE.

The expansion interface provides a parallel printer interface to suit Centronics type parallel printers. Fig. 2.1 shows how the printer cable is plugged into the logic board. The printer plug is "D" shaped and can only be inserted in one direction into the printer.

7.0 MEMORY EXPANSION.

The expansion interface allows the user to add up to 32K bytes of RAM to the system. This is done in 8K byte blocks by plugging additional IC's in sockets on the logic board. Because the MICRO-80 expansion uses the latest CMOS RAM's each 8K byte block requires only one IC and a full 32K only 4 IC's. These RAM's can be bought from MICRO-80 in RAM upgrade kits. When ordering RAM upgrades make sure to specify that it is for the MICRO-80 expansion interface as you may otherwise end up with a dynamic RAM kit to suit the old SYSTEM-80 and TRS-80 interfaces.

Fig. 10.1 shows the location of the RAM sockets on the logic board. They are numbered Z21,Z22,Z28,Z35, the table below shows the addresses to which they are decoded.

RAM IC No.	START ADDRESS.	END ADDRESS.
Z35	8000H	9FFFH
Z28	A000H	BFFFH
Z22	C000H	DFFFH
Z21	E000H	FFFFH

NOTE: If you have a TRS-80 or SYSTEM-80 fitted with 48K internal memory either through piggy backing memory IC's or through fitting an accessory keyboard memory expansion board it will be necessary to disable the MICRO-80 expansion memory buffers. The MICRO-80 expansion board provides a memory disable jumper to achieve this. The jumper is marked "X", if this jumper is bridged the RAM is enabled. If it is open the RAM is disabled (see technical section for further details).

8.0 TRS-80 COMPATIBLE OUTPUT BUS.

The logic board has a TRS-80 style output bus with most of the TRS-80 signals on it. This bus has the standard TRS-80 card edge. Any TRS-80 compatible peripheral should work from this bus. Note that this bus is unbuffered and no more than one LSTTL load should be presented to each signal on the bus.

9.Ø ADDRESS AND PORT DECODING SCHEME.

This section shows all ports and addresses decoded by the system and the function of each. See section 7.Ø for RAM addresses.

9.1 READ ADDRESSES.

ADDRESS	DIRECTION	FUNCTION.
37EØH	READ	This address reads the interrupt latch and then resets it. Data bit 7 if set means that the interrupt came from the Floppy Disk Controller. Data bit 6 if set means that the interrupt came from the 25mS clock interrupt. Note that reading this address will automatically reset the clock interrupt status bit 7 after reading but not bit 6 which comes from the FDC. (See circuit diagram).
37E8H	READ	This is the printer port status. The same information can also be read through port FDH for SYSTEM-8Ø compatibility. The bits read have the following definitions: BIT 7 - BUSY BIT 6 - PAPER EMPTY BIT 5 - SELECT BIT 4 - FAULT
37ECH	READ	FDC Status register. (See WD1771 data sheet for additional information)
37EDH	READ	FDC Track register.
37EEH	READ	FDC Sector register.
37EFH	READ	FDC Data register

9.2 WRITE ADDRESSES.

ADDRESS	DIRECTION	FUNCTION.
37EØH	WRITE	Drive/Side select latch and motor on latch. Drives Ø to 3 are selected from this address. Drive 3 or Side select can be latched depending on jumper "B" (See technical section) Whenever a 37EØ Write is decoded the MOTOR-ON signal is set, this signal will stay set for approx. 1 second when it will automatically reset. The DOS writes to this location repeatedly to keep the drive motors on during disk accesses. DØ when set = Drive Ø select. D1 when set = Drive 1 select. D2 when set = Drive 2 select. D3 when set = Drive 3 select or Side 1 select depending on logic board jumper "B".
37E8H	WRITE	Parallel printer data bus.
37ECH	WRITE	FDC Command register. (see WD 1771 data sheet)
37EDH	WRITE	FDC Track register.
37EEH	WRITE	FDC Sector register.
37EFH	WRITE	FDC Data register.

9.3 INPUT PORTS.

PORT	DIRECTION	FUNCTION.
E8H	INPUT	Read RS232 port status. D0 = RX. D5 = CD. (Low when active) D6 = DSR. (Low when active) D7 = CTS. (Low when active)
E9H	INPUT	RS232 Configuration jumpers "E". (Can also be used as general purpose input port.)
EAH	INPUT	Read UART status flags. Status bit definitions when Set: D3 = PE (Parity Error). D4 = FE (Framing Error). D5 = OE (Overrun Error). D6 = THRE (Transmitter Holding Register Empty). D7 = DR (Data Received).
EBH	INPUT	Read receiver register and reset DR (Data Received status flag).
FDH	INPUT	See 37E8H read in section 9.1.

9.4 OUTPUT PORTS.

PORT	DIRECTION	FUNCTION.
E8H	OUTPUT	UART Master Reset. An OUT (0E8H),A will reset the UART. (The data written to this port is ignored by the hardware).
E9H	OUTPUT	Program baud rate generator port. D0 to D3 program the Receive baud rate, and D4 to D7 program the Transmit baud rates. Both Transmit and Receive baudrates are latched at the same time. Select the required baud rate values from the table below, and assemble MOST and LEAST significant nibble values into a byte and send to Port E9H. 0H = 50 BAUD. 1H = 75 BAUD. 2H = 110 BAUD. 3H = 134.5 BAUD. 4H = 150 BAUD. 5H = 300 BAUD. 6H = 600 BAUD. 7H = 1200 BAUD. 8H = 1800 BAUD. 9H = 2000 BAUD. AH = 2400 BAUD. BH = 3600 BAUD. CH = 4800 BAUD. DH = 7200 BAUD. EH = 9600 BAUD. FH = 19200 BAUD.
EAH	OUTPUT	RS232 Transmit enable and Handshake latch. D0 = RTS. If this bit = 0 (reset) RTS is made active (+ve). D1 = DTR. If this bit = 0 then DTR is made active (+ve). D2 = Transmit enable. If this bit is 1 (set) then characters can be sent otherwise transmit is disabled and no characters can be sent. D3 = Parity inhibit. If set this bit will disable parity. D4 = Stop bit select. 0 = 1 Stop bit, 1 = 2 Stop bits.

D5,D6 = Word length select.

Word length	D5	D6
5 Bits	0	0
6 Bits	0	1
7 Bits	1	0
8 Bits	1	1

D7 = Parity select. If this bit is 0 parity = ODD otherwise parity = EVEN.

EBH	OUTPUT	Load transmitter data register.
FDH	OUTPUT	Parallel printer port data bus.

10.0 TECHNICAL SECTION.

This section of the manual describes the circuit diagrams and other technical information pertaining to interfacing to the expansion interface. The information in this section is mainly of use to users with knowledge of electronics, TTL logic and assembly language programming. Any interference with the logic circuits other than standard setup procedures such as configuring the RS232 port jumpers and plugging peripheral cables into the corresponding sockets will immediately void the warranty of the expansion interface.

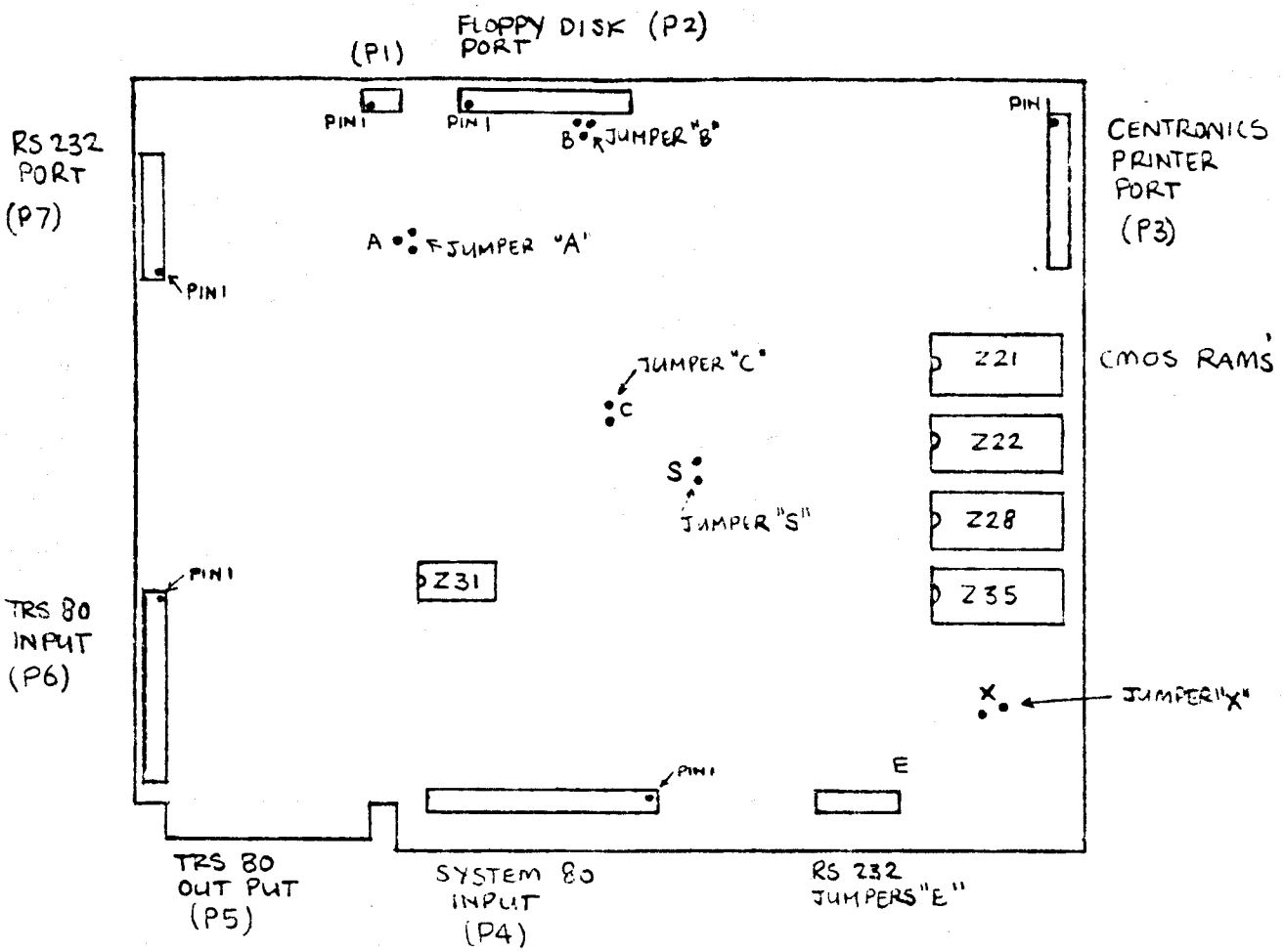


FIG 10.1

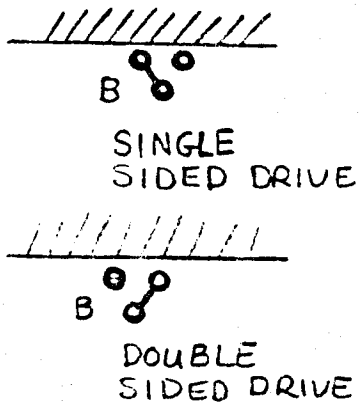
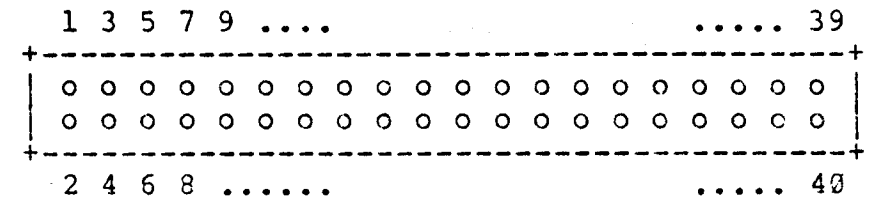


FIG 10.2

10.1 CONNECTOR SIGNAL PINOUTS.

This section shows the locations of peripheral connectors and their pinouts. For reliability reasons the MICRO-80 expansion interface has headers instead of card edges. However, the orientation of these is the same as the standard card edges. This means that existing cables can be used provided that a socket connector is clamped on instead of, or next to, the card edge connector on the cable. It is advisable however to buy new cables to suit the MICRO-80 expansion interface. Fig 10.1 shows the locations of all the sockets for the peripherals. Also note that the pin numbering convention on the RS232 socket is different from the others, this is to suit RS232 DB25 conventions.

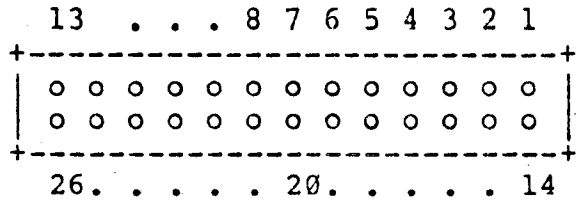
P6 TRS-80 INPUT BUS HEADER VIEWED FROM TOP.



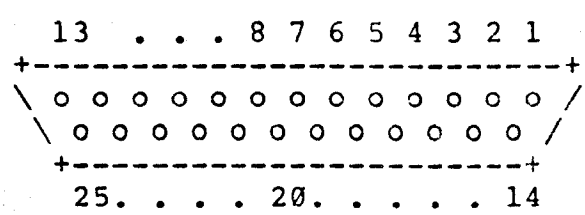
PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	MREQ* (RAS)	2	SYSRES*
3	N/C	4	A10
5	A12	6	A13
7	A15	8	GND
9	A11	10	A14
11	A8	12	OUT*
13	WR*	14	INTAK*
15	RD*	16	N/C
17	A9	18	D4
19	IN*	20	D7
21	INT*	22	D1
23	TEST*	24	D6
25	A0	26	D3
27	A1	28	D5
29	GND	30	D0
31	A4	32	D2
33	WAIT*	34	A3
35	A5	36	A7
37	GND	38	A6
39	GND	40	A2

(N/C = NO CONNECTION, * = ACTIVE LOW)

P7 RS232 PORT PCB header viewed from top.



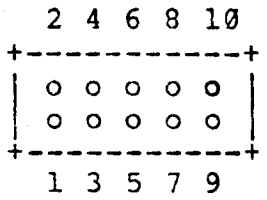
Female DB25 pinout on adaptor cable. (Available from Micro-80)



PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	N/C	2	TX
3	RX	4	RTS
5	CTS	6	DSR
7	GND	8	CD
9	N/C	10	N/C
11	N/C	12	N/C
13	N/C	14	N/C
15	N/C	16	N/C
17	N/C	18	N/C
19	N/C	20	DTR
21	N/C	22	N/C
23	N/C	24	N/C
25	N/C	26	N/C

(N/C = NO CONNECTION, * = ACTIVE LOW)

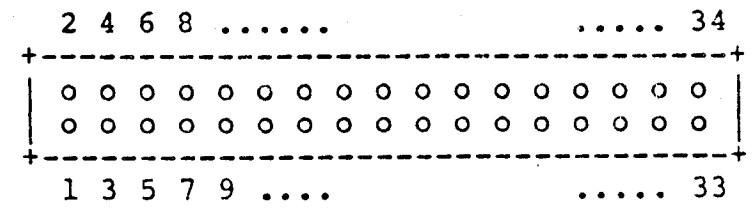
P1 EXTERNAL DATA SEPARATOR SOCKET. Viewed from top.



PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	RAW	2	PHØ (2 Mhz)
3	GND	4	GND
5	VCC	6	VCC
7	N/C	8	N/C
9	DAT	1Ø	CLK

(N/C = NO CONNECTION, * = ACTIVE LOW)

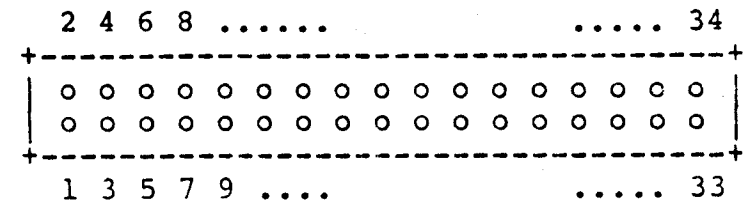
P2 FLOPPY DISK BUS. Viewed from top.



PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	GND	2	N/C
3	GND	4	N/C
5	GND	6	DRIVE 3 SELECT*
7	GND	8	INDEX*
9	GND	10	DRIVE Ø SELECT*
11	GND	12	DRIVE 1 SELECT*
13	GND	14	DRIVE 2 SELECT*
15	GND	16	MOTOR-ON*
17	GND	18	DIR SELECT
19	GND	20	STEP*
21	GND	22	WRITE DATA*
23	GND	24	WRITE GATE*
25	GND	26	TRACK ZERO*
27	GND	28	WRITE PROT*
29	GND	30	READ DATA*
31	GND	32	SIDE SELECT
33	GND	34	N/C

(N/C = NO CONNECTION, * = ACTIVE LOW)

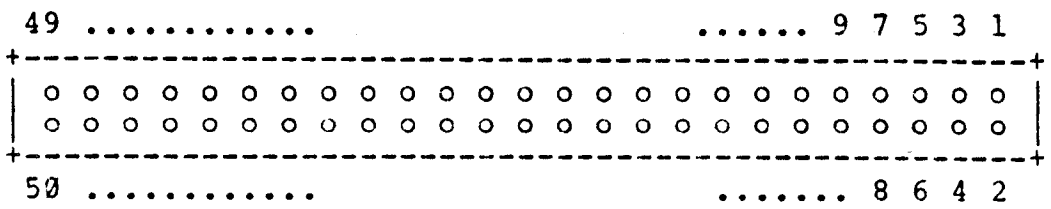
P3 PARALLEL PRINTER BUS. Viewed from top.



PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	STROBE*	2	GND
3	PDØ	4	GND
5	PD1	6	GND
7	PD2	8	INDEX*
9	PD3	1Ø	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	N/C	2Ø	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	N/C
27	N/C	28	FAULT
29	N/C	3Ø	N/C
31	N/C	32	N/C
33	N/C	34	N/C

(N/C = NO CONNECTION, * = ACTIVE LOW)

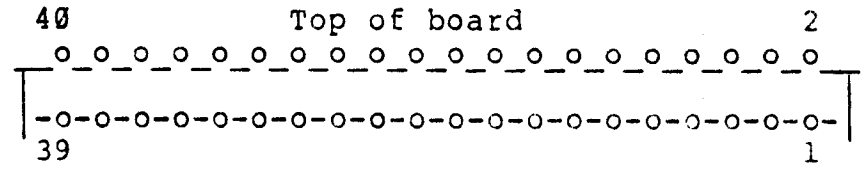
P4 SYSTEM-80 INPUT BUS. Viewed from top.



PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	GND	2	GND
3	A7	4	A6
5	A5	6	A4
7	A1	8	A3
9	A2	10	A0
11	D5	12	D2
13	N/C	14	D1
15	D0	16	D3
17	D7	18	D6
19	N/C	20	D4
21	A15	22	A8
23	A14	24	A9
25	N/C	26	A10
27	A13	28	A11
29	A12	30	N/C
31	INT*	32	N/C
33	N/C	34	N/C
35	N/C	36	N/C
37	WAIT*	38	IORQ*
39	N/C	40	WR*
41	RD*	42	TEST*
43	MREQ*	44	TEST*
45	N/C	46	RESET*
47	N/C	48	N/C
49	GND	50	GND

(N/C = NO CONNECTION, * = ACTIVE LOW)

P5 TRS-80 OUTPUT BUS. (Card edge)



PIN No. - SIGNAL NAME		PIN No. - SIGNAL NAME.	
1	MREQ* (RAS)	2	SYSRES*
3	N/C	4	A10
5	A12	6	A13
7	A15	8	GND
9	A11	10	A14
11	A8	12	OUT*
13	WR*	14	INTAK*
15	RD*	16	N/C
17	A9	18	D4
19	IN*	20	D7
21	INT*	22	D1
23	TEST*	24	D6
25	A0	26	D3
27	A1	28	D5
29	GND	30	D0
31	A4	32	D2
33	WAIT*	34	A3
35	A5	36	A7
37	GND	38	A6
39	GND	40	A2

(N/C = NO CONNECTION, * = ACTIVE LOW)

10.2 BUFFERING.

The expansion interface is fully buffered with TTL type line drivers. The address buffers are in the RAM section and are numbered Z37 and Z36 (Sheet 3) they are permanently enabled as the address lines are needed all the time. These buffers present only 1 LSTTL load to the keyboard whilst they provide the entire expansion board with addresses.

The TRS-80 & SYSTEM-80 address and control signals are so degraded because of insufficient buffering in the keyboard unit that pull down resistors have been used to provide an impedance match to the signals traveling down the interconnecting ribbon cable. This stops reflections and ringing. The signals are then further cleaned up by the hysterisis of the buffers. The control signals RD*, WR* and MREQ* are buffered by Z32.

10.3 ADDRESS DECODING.

Address decoding is split into two sections, namely RAM and I/O device decoding. The expansion interface uses the latest technology CMOS RAMS, these RAMS have 8 Kbytes of RAM per chip. This means that four areas have to be decoded, namely 8000H to 9FFFH, A000H to BFFFH, C000H to DFFFH and E000H to FFFFH to supply each chip with an enable signal. If you study the addresses of the four blocks you will notice that only three address lines need to be decoded namely A13, A14 and A15 to get the correct RAM chip enable signals. This is accomplished by Z27 which is a three to eight line decoder (sheet 4). Only four outputs of this decoder are used by the RAM's, this conveniently leaves us one of the other four outputs namely "1" (pin 14), which decodes 2000H to 3FFFH. This is within the range of the TRS-80 I/O addresses which have to be decoded. The I/O device addresses range from 37E0H to 37EFH. This means that apart from the above mentioned signal we also have to process A2 to A12 to further decode the correct addresses. (A0 and A1 are decoded by the FDC directly and should be left alone). All this is accomplished by Z34, Z33, Z39 and Z26. Z26 is a dual two to four line decoder, half of which is used to generate Read enables and the other is used for Write enables. Note that address 37E4H was used for dual cassette signals in the original TRS-80 interface. The MICRO-80 interface does not implement dual cassettes as this feature is no longer supported in later model TRS-80 ROM's and the SYSTEM-80 already has a dual cassette interface inbuilt. (See also RAM section for decoding on databus buffer)

10.4 PORT DECODING.

The only ports that need to be decoded are for the RS232 section and for the SYSTEM-80 printer port. This means that we need to decode ports E8H to EBH and port FDH. This is done with Z19, Z43 and Z20. Z20 is a four to sixteen line decoder. Half is used for input port decoding and the other half is used for output port decoding, this is achieved by feeding the BIN* signal (see sheet 1) which is a Buffered IN* from the TRS-80, into the A3 input of the decoder. This effectively splits the decoder in half. Note that the decoding scheme is such that the ports are in fact dual decoded. Port decode signal PDFDOUT* and PDFDIN* for instance goes active for either port EDH and FDH but since port EDH is not used this does not matter.

10.5 FLOPPY DISK CONTROLLER.

When the original TRS-80 expansion interface was designed the only commonly available Floppy Disk Controller (FDC) was the WD1771. Which is a single density 8 or 5 1/4 inch FDC. The bootstrap loader and DOS have all been written to suit this chip which means that any new hardware designs have to continue to use this device. This is somewhat unfortunate as the later generation FDC's from Western Digital have Single and Double density capability and have an onboard phase locked loop data separator (i.e. WD2791). That is why a double density adaptor is needed for the TRS-80 containing the WD1771 and one of the newer chips for double density operation. As far as data separation is concerned there was a problem with the early WD1771 FDC's and early 5 1/4 inch disk drive units with reliablity. This was partly overcome by plugging in an optional data separator. This situation however is now no longer as critical as it used to be. The later model Japanese made 40 track disk drives (Shugart slimline, Mitsubishi, etc.) are much improved as are the newer FDC chips due to improved manufacturing techniques. For this reason the standard MICRO-80 expansion interface does not have an external data separator. The double density adaptor however has a phase locked loop data separator (available from MICRO-80 as an optional extra) and for those running older disk drives an optional plug in data separator is available.

CIRCUIT DESCRIPTION.

Here we will discuss the FDC circuit with the exception of the Interrupt section which is discussed in section 10.7. See also the section in the user manual on the address decoding scheme for the FDC. The WD1771 takes care of most of the interface signals required for the floppy disk drives. The interface allows for up to four floppy disk drives to be connected to it. These drives are daisy-chained on a common cable. Before the FDC can be made to access a disk drive the required drive must be selected. This is accomplished with a latch (Z11) which drives some open collector buffers to suit the floppy disk drive bus. The active low outputs of this latch (Z11) are connected to a four input NAND gate Z19. As soon as any of the drive select outputs goes low the output of Z19 goes high. This supplies the FDC chip with the HLT and RDY (Head load and Ready) inputs. When a Write to 37E0H is executed to select a drive it also triggers a monostable Z3 which causes the MOTOR-ON signal to go active for at least one second. Repeated writes to 37E0H are required to keep the motors running and the drive selected for more than one second. If the monostable times out, it will also reset latch Z11 through the CLR input (Z11 pin 1) thereby automatically deselecting the drives. The

only other part of the circuit to be described here are the buffers Z24 and Z25. They are simply inverting buffers connected for bidirectional operation and are decoded to 37ECH.

FDC JUMPER OPTIONS.

Jumper "B" is provided to modify the expansion interface to suit single or double sided disk drives. As standard it is set up for single sided operation. If double sided operation is required jumper "B" has to be cut and a small piece of wire wrap wire soldered in place. Jumper "B" is located just below the Floppy Disk header, see Fig 10.2 for more details. Note: This jumper is valid only if a straight through cable is used for the disk drives with no teeth missing in the drive card-edge connectors and no signals crossed-over on the diskdrive card-edges.

When the TRS-80 was designed, double-sided disk drives where not available and therefore the SIDE-SELECT signal was not used on early drives. Neither the TRS-80 nor SYSTEM-80 expansion interfaces provide a signal for SIDE-SELECT to the disk drive due to this. When double sided (Dual head) drives became available a choice had to be made on how to support these drives by the authors of the various DOS's. The only logical way was to use the DRIVE-SELECT 3 output as the SIDE-SELECT signal. This limits the maximum number of double-sided (dual-head) drives that can be connected to the system to three instead of four. The SIDE-SELECT signal is on pin 32 of the disk drive card-edge and the DRIVE-SELECT 3 signal is on pin 6. Hence the need for Jumper "B" (See sheet 2, top right corner) which allows the user to direct the DS3 signal to either pin 6 (Drive-Select 3) for single-sided operation or pin 32 (Side-Select) for double-sided operation.

10.6 RS232 SECTION.

The RS232 section is functionally almost identical to the TRS-80 version, thereby removing yet another incompatibility between the SYSTEM-80 and the TRS-80 when the MICRO-80 expansion interface is used with a SYSTEM-80. It is based on a TR1602 type UART (See sheet 1). Z29 is used to buffer the data bus and Z17 buffers the handshake signals from the RS232 level converters Z16. Since this type of UART does not provide inputs or outputs for the RS232 handshake signals, they are handled by a buffer and latch. Z9 latches the output handshake signals for the RS232 port and Z8 converts the TTL levels to RS232 levels. TTL levels are 0 to +5 volts, whereas RS232 levels used here are -12 to +12 volts, hence the need for Z8 and Z16. Z43 is the baud rate generator and supplies both the receive and transmit clocks to the UART (see port decoding scheme section for details on programming the baud rates).

Jumper area "E" has been provided for compatibility to existing RS232 software that needs to read the configuration switches. If it is not required for this purpose the jumper blocks can be removed from the pins and a standard 16 PIN socket connector can be plugged into this header to provide an eight bit input port. This could be used for any purpose such as to connect a switch type joystick or what ever. The pins are numbered 1 to 8 on the logic board, where pin 1 is data bit 7 and pin 8 is data bit 0, all the pins on the top row are connected to GND and all input pins are pulled up to VCC through 4K7 resistors.

10.7 CLOCK AND INTERRUPTS.

The expansion interface provides the TRS-80 with an interrupt every 25mS. This is provided by the clock circuit consisting of Z1, Z2, Z5, Z13, Z14 and Z6. Z1 is used as a crystal controlled oscillator and feeds counters Z2 and Z5. Z2 generates the necessary clock signals for the FDC and external data separator. Z5, Z13 and Z14 divide the 4Mhz clock until it is reduced to 40Hz for the 25mS clock interrupt pulse. Besides the clock circuit the FDC can also generate an interrupt. To allow the system to tell which device (clock or FDC) has interrupted, either D6 or D7 will be high if address 37E8H is read (Interrupt status). D6 will be high if the FDC is interrupting and D7 if the 25mS clock is interrupting. All this is achieved by Z12. Note that the INT* line is of Open Collector type to allow multiple outputs to be wire ORed together.

The FDC can operate with or without interrupts. At the completion of a command, both a status bit is set in the FDC status register and an interrupt is generated. This means that the FDC can be polled to determine if it has finished a command or the processor can be put in HALT mode to wait for an interrupt. If the FDC interrupt part of the circuit is not functioning strange faults can develop. The faults will vary from DOS to DOS. To start with, the bootstrap loader in ROM does not use the interrupts and would function as normal. However the initialization routine which is read from sector 1 track 0 may or may not work depending on whether it uses interrupt or polled mode. Situations have occurred where one DOS would boot but another would not. Or a DOS would boot but certain functions or utilities would not work properly. Whenever strange faults like these develop always check whether the interrupt circuit is functioning.

10.8 PARALLEL PRINTER INTERFACE.

The printer interface (sheet 4) is rather simple. It consists of a monostable Z3 to generate the STB* pulse which is about 1 to 1.5 uS long and a latch Z7 to latch the data on the printer bus. A buffer Z15 is used to read the printer status lines. Z43 causes the printer port to respond to either port FDH for SYSTEM-80 compatibility or address 37E8H for the TRS-80.

10.9 MEMORY CIRCUIT.

The MICRO-80 expansion interface uses the latest technology CMOS RAMS, these RAMS have 8 Kbytes of RAM, 8 bits wide per chip. This means that the 32Kbytes required on the expansion interface need only four chips. Memory can be upgraded one chip or 8K at a time. The advantage of these chips are many: Low power consumption, less susceptability to power supply spikes, very high speed (150 nS access) and only a single supply voltage is required.

The memory data bus buffer Z40 is enabled by ANDing an inverted MREQ signal and A15 together. This means that the buffer is enabled for addresses 8000H to FFFFH, which covers the 32K range of the CMOS RAMs.

Note that the chip enable pin 19 of Z40 has a pull up resistor and a jumper marked "X" connected to it. If jumper "X" is cut, the memory buffer is permanently disabled. This is done because some users have expanded their memory to 48K inside the keyboard unit. See Fig 10.1 for jumper "X" location.

10.10 SYSTEM-80 TO TRS-80 CONVERSION CIRCUIT.

The expansion board internally has the same control signals as the TRS-80 expansion interface. To make the interface compatible with both the SYSTEM-80 and the TRS-80 some extra circuitry is required to change some of the SYSTEM-80 signals to TRS-80 signals. This circuit consists merely of five OR gates contained in Z31 and Z33. The TRS-80 compatible signals that this circuit provide are RD*, WR*, IN*, OUT* and INTAK*.

If you look at sheet 4 you will notice that the output signals generated by the OR gates are common with the signals coming in on the TRS-80 bus. To avoid bus contention several measures have been taken. Firstly Z31 is socketed and should be REMOVED if the interface is to be used with a TRS-80. Secondly a jumper marked "S" is provided and should be cut open for TRS-80 use. Conversion from SYSTEM-80 to TRS-80 compatibility is therefore a simple matter. See Fig 10.1 for location of Z31 and Jumper "S".

10.11 POWER SUPPLY.

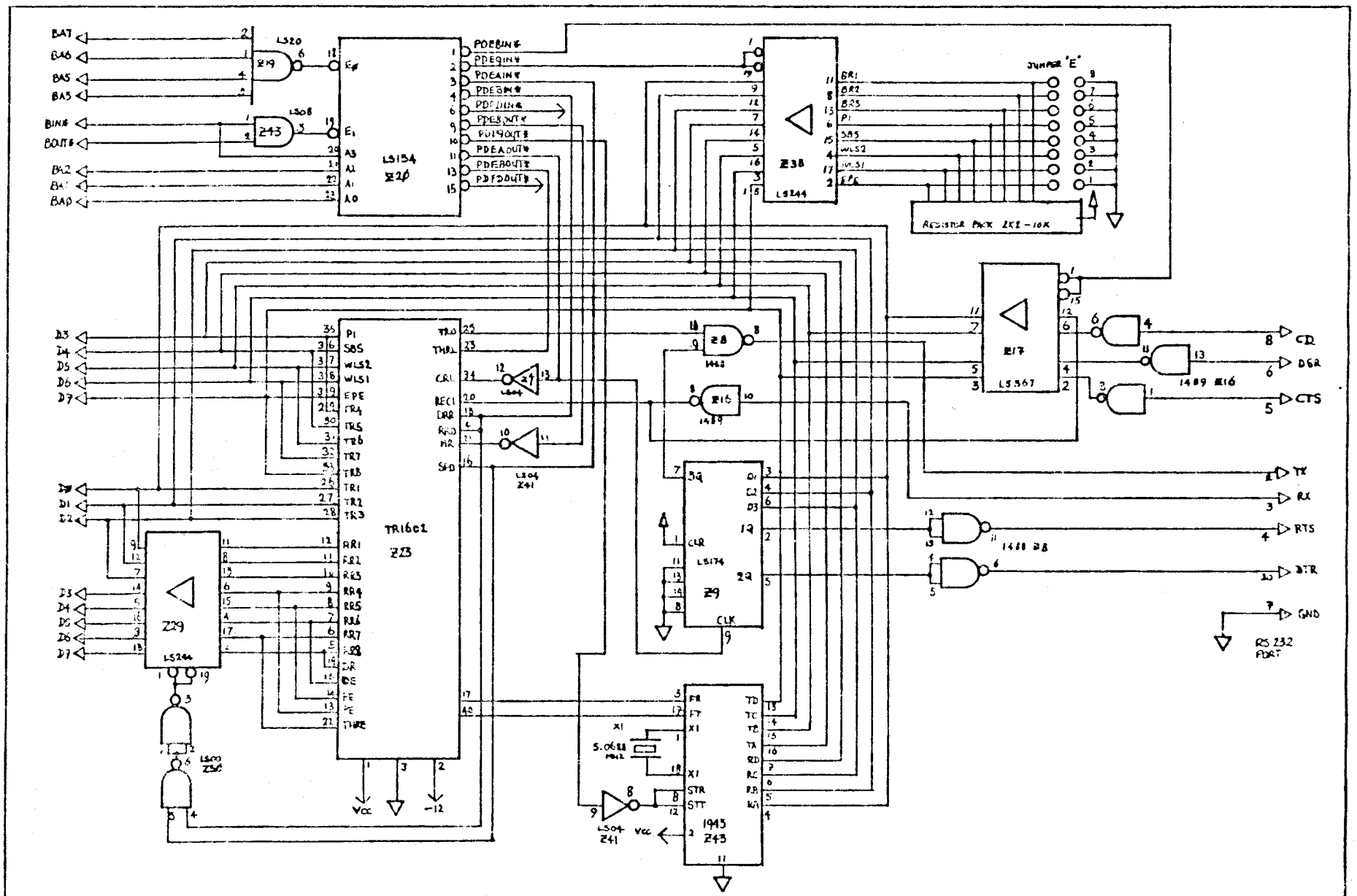
The power supply in the expansion unit is a general purpose switchmode unit. It supplies 4 different voltages for the expansion interface and disk drives namely +5V, -5V, +12V and -12V. The +5V (VCC) supply is used by almost all the chips on the board and all TTL chips. The -5V supply is used only by the floppy disk controller. The +12V and -12V supplies are used by the RS232 driver circuits and the floppy disk controller.

The interface power supply has the following ratings:

Input: 185-260Vac 50Hz. Fuse protected.

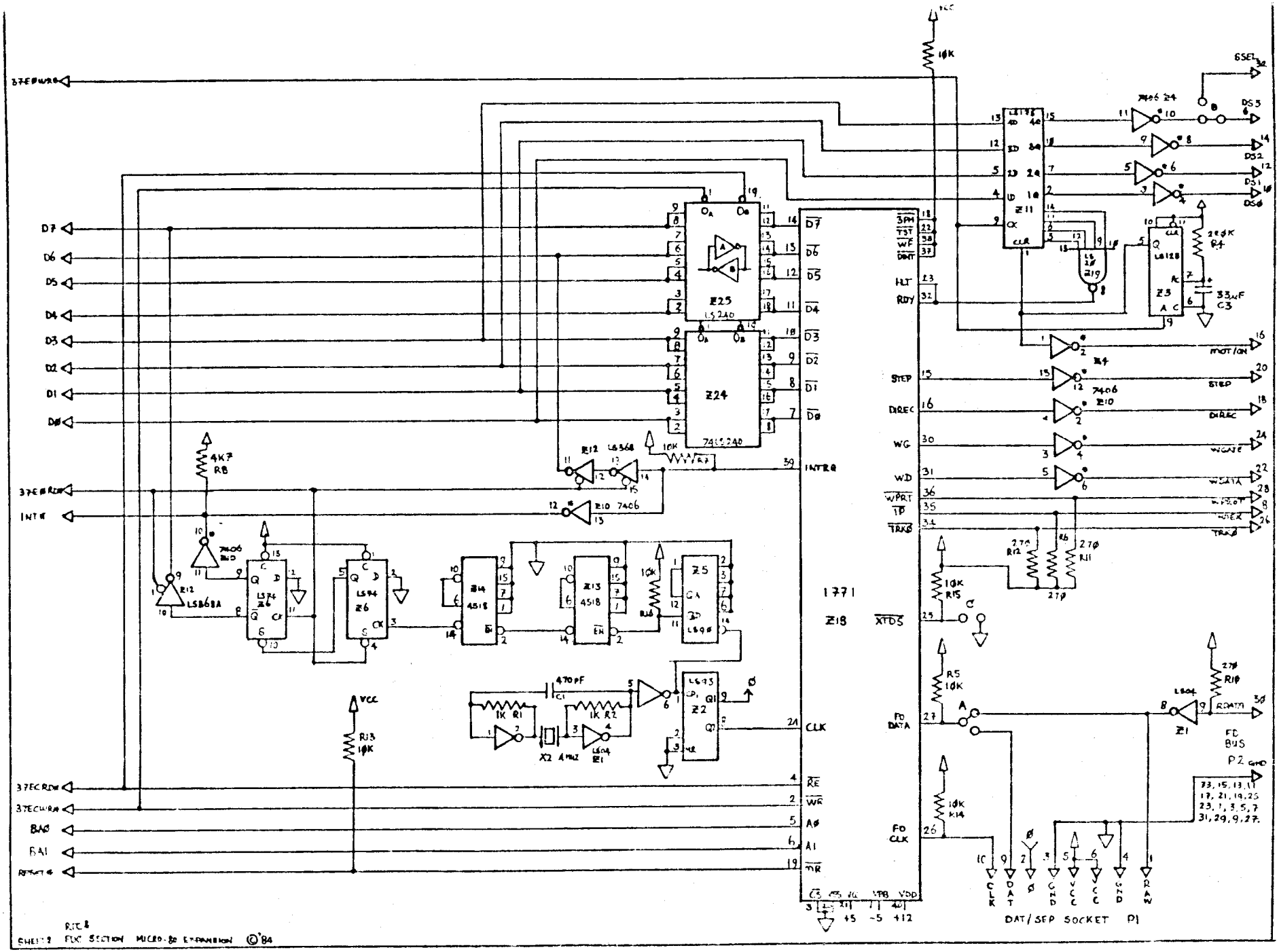
Outputs:

+5V dc.	5A.
+12V dc.	4A.
-5V dc.	500mA Max.
-12V dc.	500mA Max.



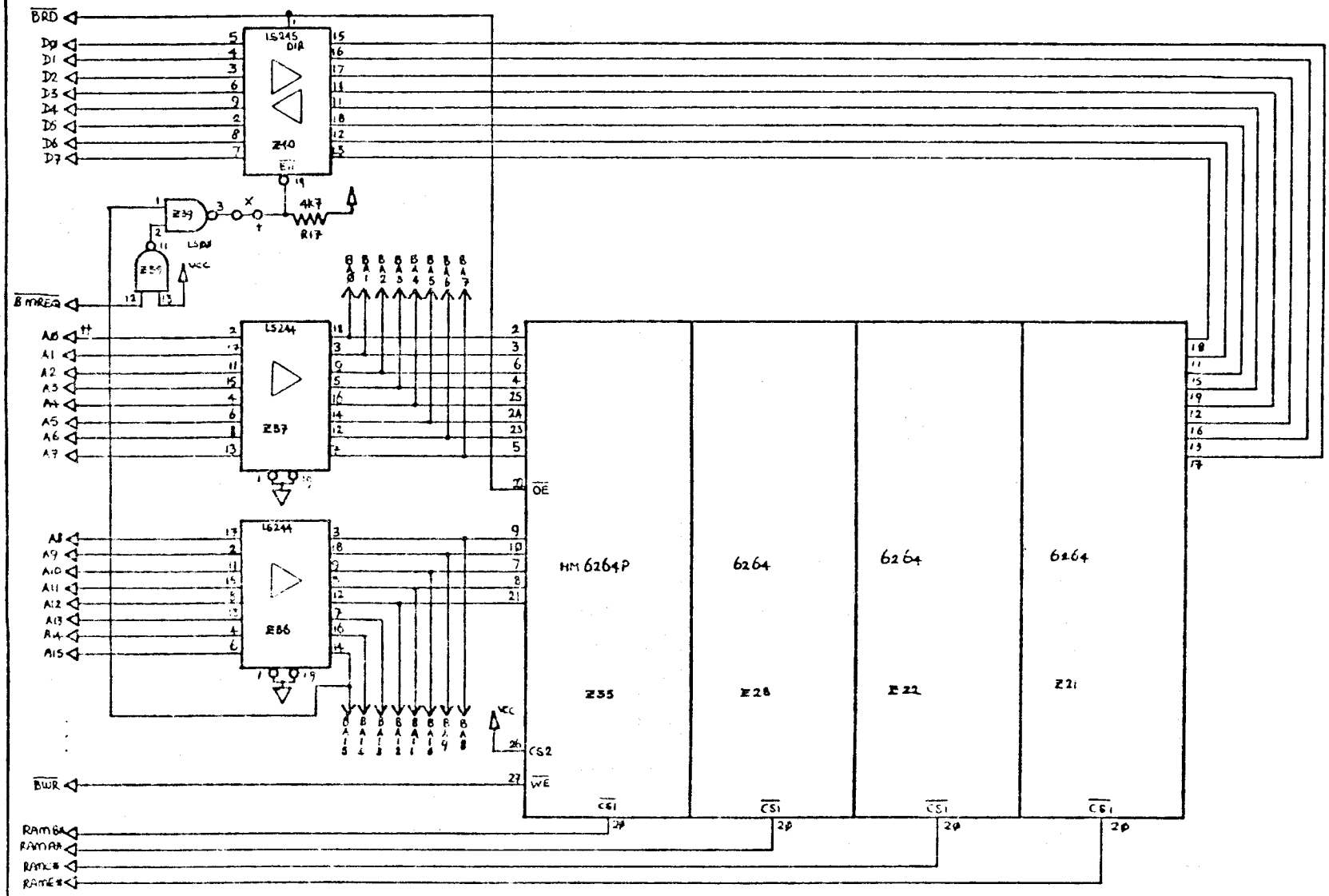
PORT DECODE &

SHEET 1 RS232 MICRO 80 EXPANSION



R1C 8

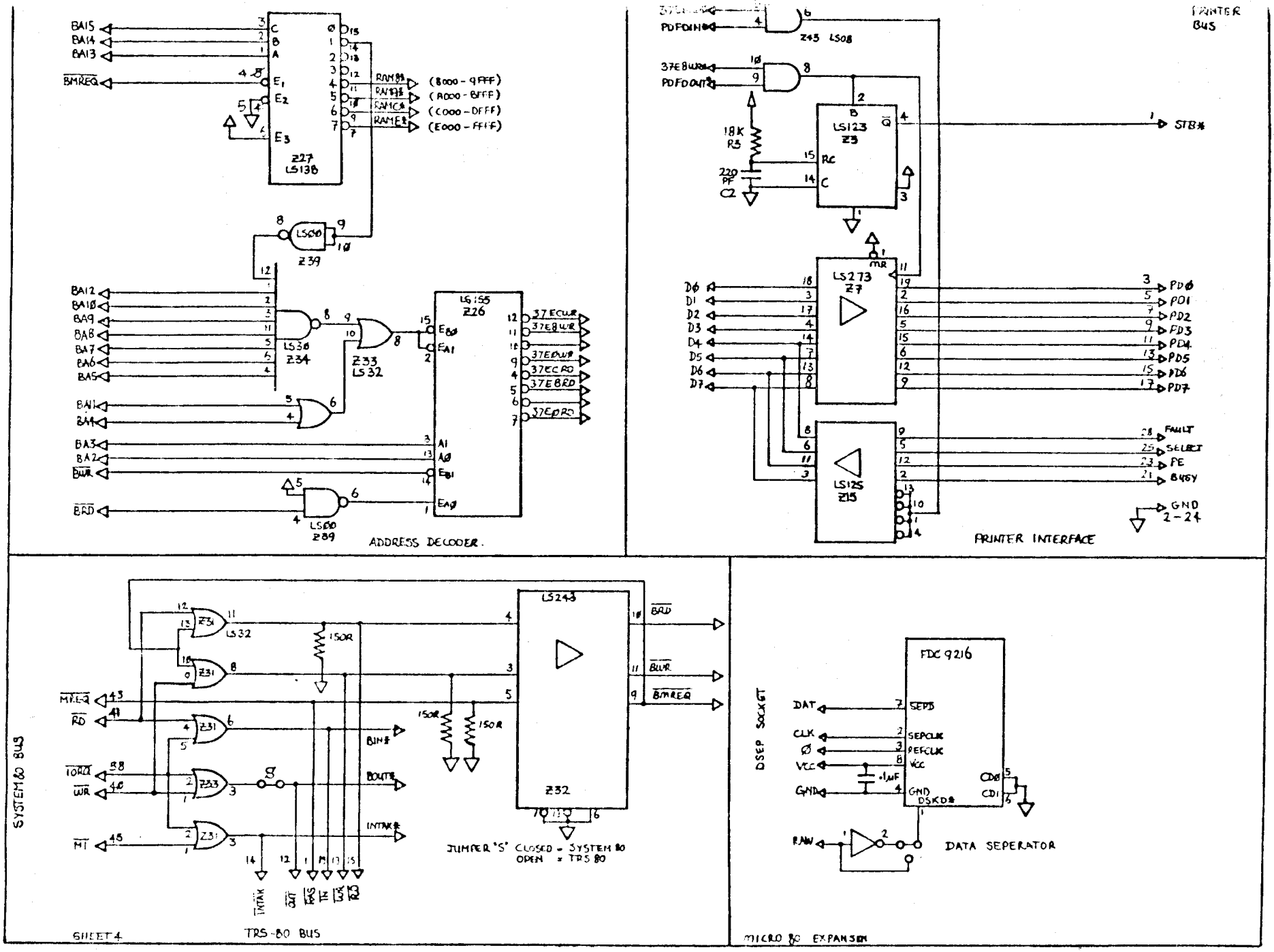
SHEET 2 FDC SECTION MICRO-80 EXPANSION ©'84

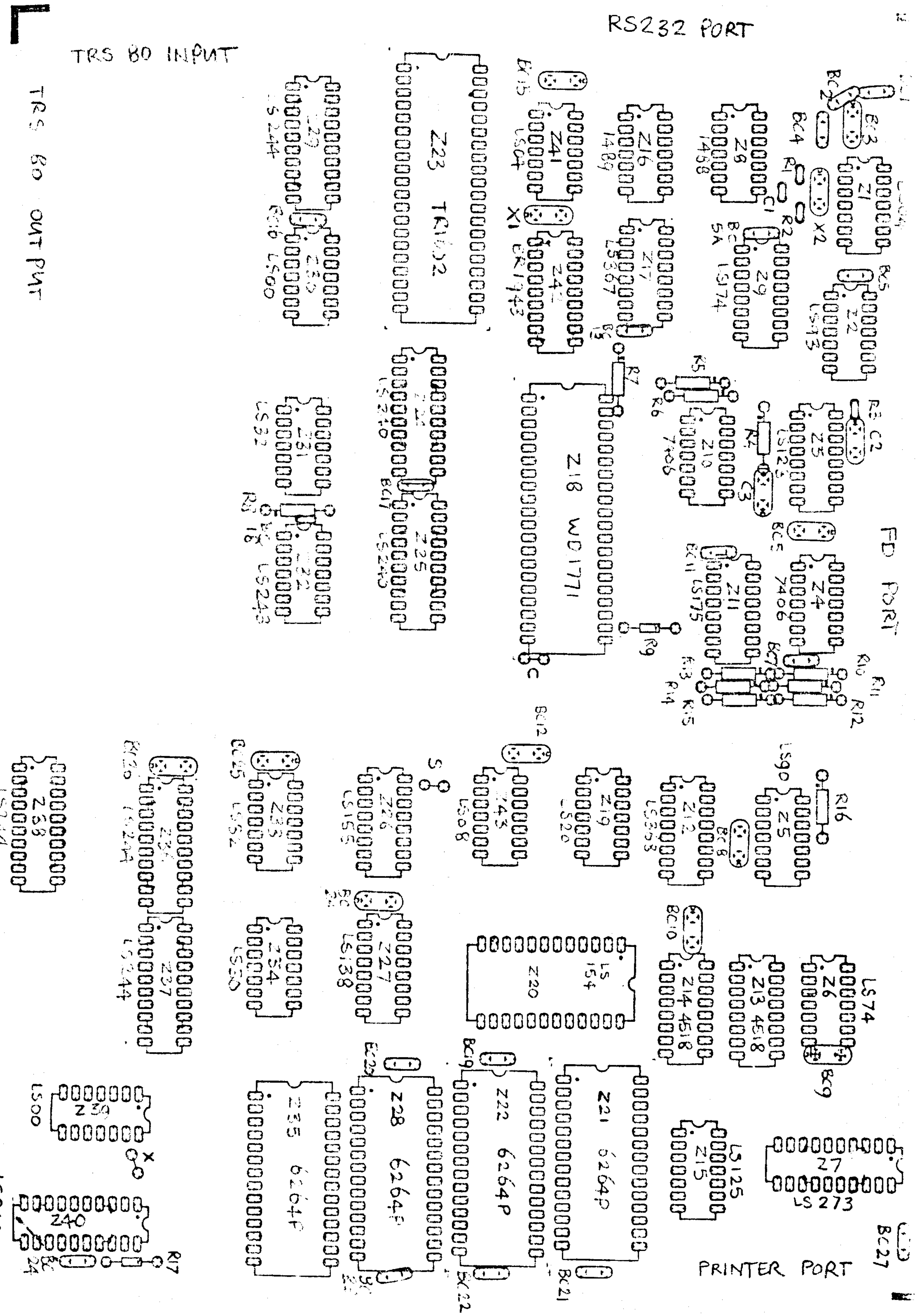


† JUMPER X - CLOSED - RAM ENABLED
OPEN - RAM DISABLED

†† ALL ADDRESS LINES HAVE 150R PULL DOWN RESISTORS ON THEM

SHEET 3 RAM & BUFFER SECTION — MICRO 80 EXPANSION


BAI5
BAI4
BAI3
BMREQ
Z27
LS138
RAM8
RAM9
RAMA
RAMB
(8000 - 9FFF)
(A000 - BFFF)
(C000 - DFFF)
(E000 - FFFF)
Z39
LS00
BAI2
BAI0
BA9
BA8
BA7
BA6
BA5
LS38
Z34
Z33
LS32
LS155
Z26
37ECWR
37E8WR
37EDWR
37ECRD
37EBRD
37EDRD
BA1
BA4
BA3
BA2
BWR
BRD
Z89
ADDRESS DECODER.
PDFDIN
Z45 LS08
37E8WR
PDFDOUT
18K
R5
220
PF
C2
LS123
Z3
STB*
MR
LS273
Z7
D0
D1
D2
D3
D4
D5
D6
D7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
LS125
Z15
FAULT
SELECT
PE
BUSY
GND
2-24
PRINTER INTERFACE
SYSTEM 80 BUS
MREQ
RD
IORQ
WR
M1
Z31
Z33
Z32
LS32
150R
BINR
BOUTR
INTAKR
LS243
BRD
BWR
BMREQ
JUMPER 'S' CLOSED = SYSTEM 80
OPEN = TRS 80
INTAK
WR
RD
TRS-80 BUS
SHEET 4
DSEP SOCKET
FDC 9216
DAT
CLK
Ø
VCC
GND
SEPD
SEPCLK
REFCLK
VCC
GND
DSKD*
CD0
CD1
.1μF
R/W
DATA SEPERATOR
MICRO 80 EXPANSION



RS232 PORT
TRS 80 INPUT
TRS 80 OUTPUT
SYSTEM 80 INPUT
FD PORT
PRINTER PORT
Z23 TR1602
Z18 WD1771
Z21 6264P
Z22 6264P
Z28 6264P
Z35 6264P
Z20 LS154
Z7 LS273
Z6 LS74
Z13 4518
Z14 4518
Z15 LS125
Z4 7406
Z11 LS175
Z9 LS174
Z41 LS04
Z42 ER1443
Z16 1489
Z8 1488
Z37 LS244
Z38 LS244
Z39 LS00
Z40 LS244
Z27 LS138
Z43 LS08
Z12 LS393